Product Information

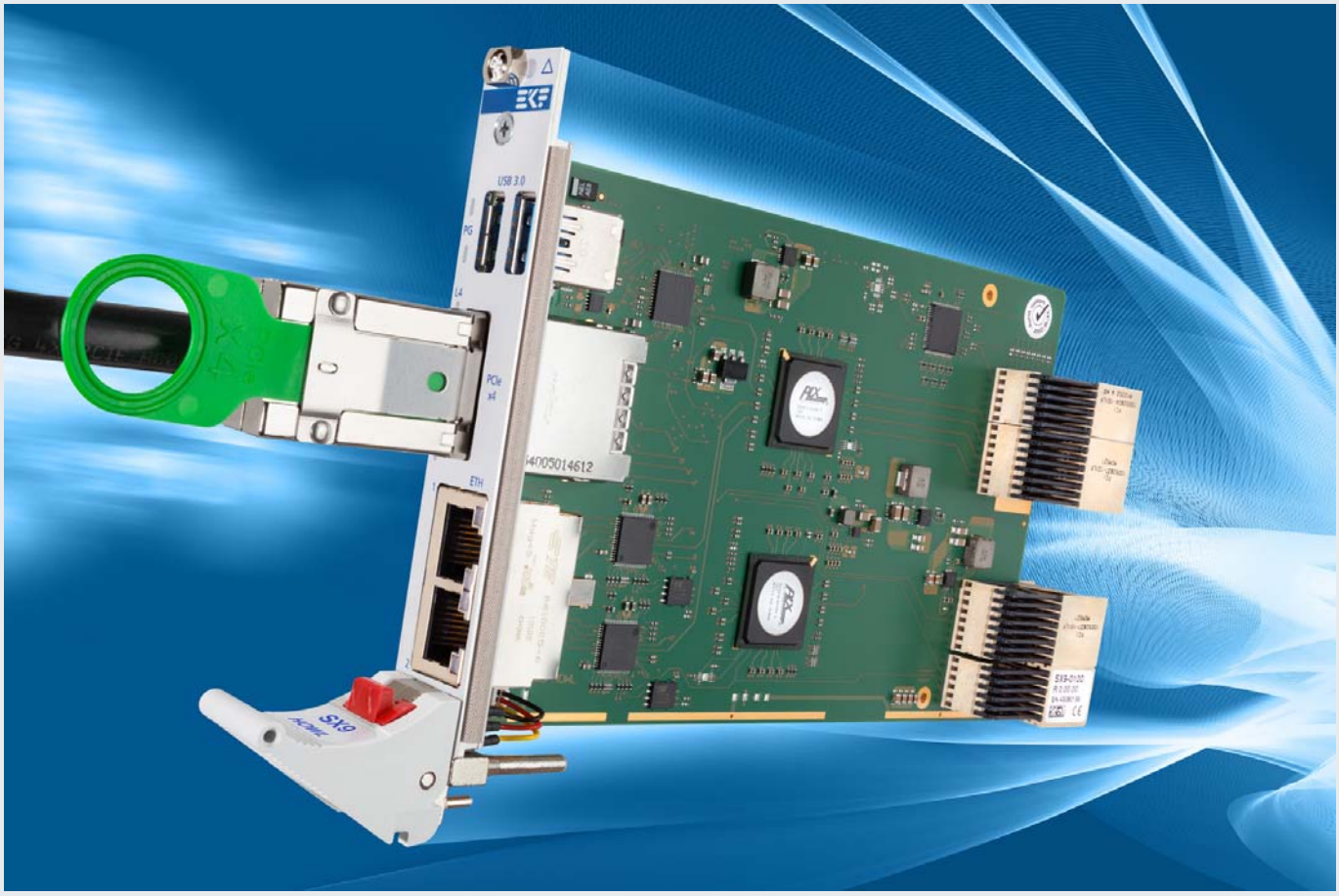
SX9-HOWL

CompactPCI® Serial • PCI Express® External Cabling

Target Side Adapter

Enables PCIe Based Peripheral Cards in a CompactPCI® Serial Target System

Document No. 7134 • 19 December 2017



General

Most computer systems are based on the PCI Express® standard as a high speed backbone for interconnection of peripheral components with a host CPU. Typically all PCI Express® based devices are located closely in a common enclosure.

The PCI-SIG PCI Express® External Cabling Specification addresses extended applications, such as split-systems or I/O expansion by means of a suitable copper cable, available e.g. for a x4 PCI Express® link, up to 7m length. When used with an AOC (Active Optical Cable), distances of up to 300m can be bridged between host and target systems.

The SX9-HOWL is a target system adapter card for PCIe x4 external cabling. The SX9-HOWL fits into the backplane system slot of a CompactPCI® Serial target system. Two on-board packet switches are used to replicate eight PCI Express® links across a CompactPCI® Serial backplane. Thus, up to eight PCIe based CompactPCI® Serial peripheral slot cards in a target system can be controlled by a remote host system CPU, with a maximum transfer rate of 20Gbps.

As an option, the SX9-HOWL is available with additional front panel I/O (2 x RJ45 GbE, 2 x USB 3.0).

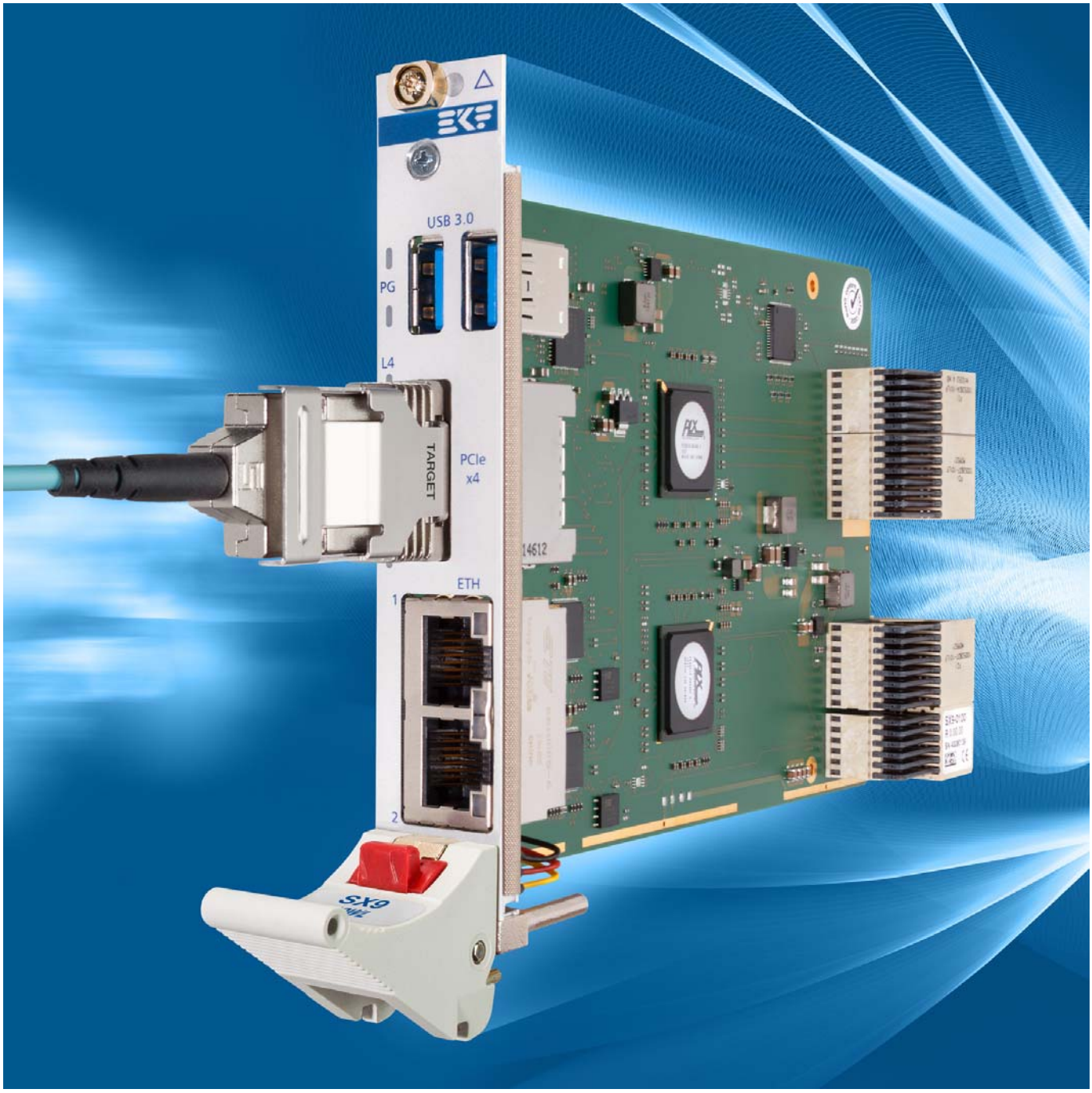
System Integration

The SX9-HOWL allows to control a CompactPCI® Serial target (downstream) system by a remote host CPU via PCI Express® external cabling. The host (upstream) system may be any computer with a PCI Express® external cabling adapter, not necessarily a CompactPCI® Serial system.

Being mainly a powerful PCI Express® packet switch, the SX9-HOWL is organized similar to a CompactPCI® Serial system slot controller card, however restricted to the PCI Express® resources of the CompactPCI® Serial backplane.

The SX9-HOWL is linked to the host system by a PCI Express® x4 front panel cabling connector (upstream), and delivers eight PCI Express® links to its backplane connectors (downstream), for up to eight CompactPCI® Serial peripheral cards in a target system. Three links/slots on the CompactPCI® Serial backplane are organized as x4, the other are single lane connections.

Hence, PCI Express® based devices in the target system can be controlled by the remote host system CPU in an identical manner as its local resources.



SX9-HOWL w. AOC (Active Optical Cable)

Feature Summary

- PCI Express® external cabling target side adapter
- PICMG® CompactPCI® Serial (CPCI-S.0) system slot controller (PCIe resources only)
- Single Size Eurocard 3U 4HP 100x160mm²
- cPCI-S Backplane connectors P1, P2, P4, P5 for 8 PCI Express® links
- Peripheral slots organized x4/x4/x4/x1/x1/x1/x1/x1

- *PCI Express® External Cabling Specification* x4 connector 38-pos. (front panel)
- Suitable for CompactPCI® Serial target systems to be controlled by a remote host
- Split-systems, hybrid systems, or system expansion applications
- Suitable for any host system with PCI Express® x4 external cabling host adapter
- Copper cable assemblies 0.5m to 7m length available
- Active optical cable assemblies (AOC) up to 300m length available
- PCIe Gen2 x 4 allows for up to 20Gbps bandwidth

- 2 x Gen2 PCI Express® 16-port/16-lanes packet switches on-board
- Option PCIe to dual-port USB 3.0 controller (front panel receptacles)
- Option 2 x Intel® I210 PCIe to Gigabit Ethernet controller (front panel RJ45)

- Long term availability
- Designed & manufactured in Germany
- ISO 9001 certified quality management
- Rugged solution (coating, sealing, underfilling on request)
- RoHS compliant 2002/95/EC
- Commercial and industrial temperature range
- Humidity 5% ... 95% RH non condensing
- Altitude -300m ... +3000m
- Shock 15g 0.33ms, 6g 6ms
- Vibration 1g 5-2000Hz
- MTBF 32 years
- EC Regulations EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1)

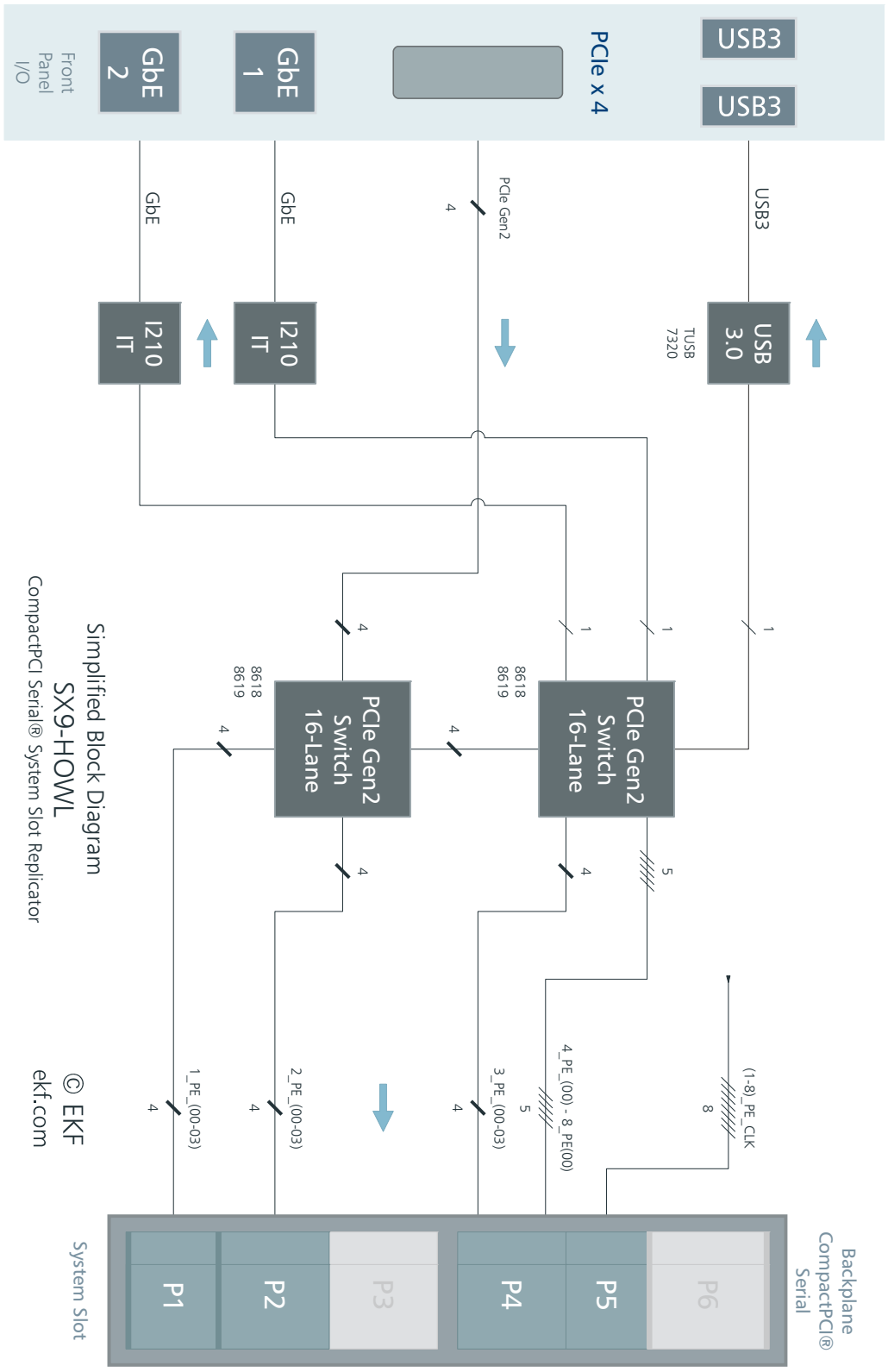
Theory of Operation

The SX9-HOWL must be inserted into the system slot of the CompactPCI® Serial target system. The PCIe x4 link derived from the front panel cabling connector is distributed across a 16-lane Gen2 packet switch to the backplane connectors P1/P2 (responsible for the CompactPCI® Serial backplane peripheral slots 1/2), and feed into a secondary 16-lane switch, which in turn is wired to the backplane connector P4 (peripheral slots 3-8). Three PCIe lanes are reserved for the optional on-board USB 3.0 controller, and another two Gigabit Ethernet controllers.

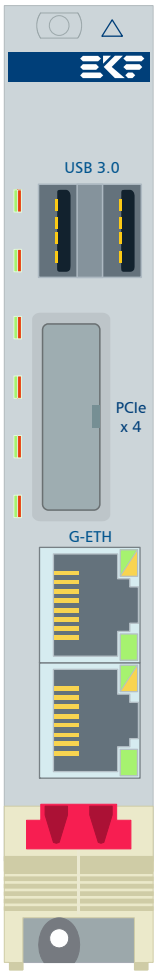
A PCI Express® zero delay clock buffer is wired to the backplane connector P5. The PCIe clock source will be either derived from the PCIe external cabling connector, or can be generated locally (dual clocking), as an optional capability for systems in which the upstream (host) devices are operating in a spread spectrum clocking (SSC) environment, while the downstream (target) links require constant frequency clocking (CFC). If possible, spread spectrum should be disabled on the host side, since it would not be compliant with active optical cable assemblies.

SX9-HOWL w. Copper Cable Assembly

Block Diagram



Front Panel



SX9-HOWL
System Slot
Replicator

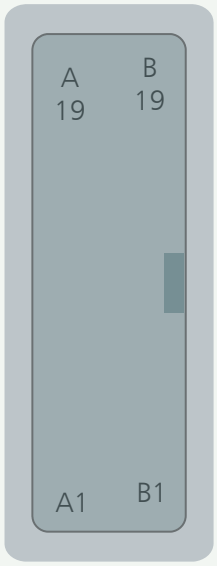
LEDs assigned to particular PCI Express® lanes:
LED off - no PCIe link established for this lane *
LED on - PCIe Gen2 link established
LED blinking - PCIe Gen1 link established

* As result of the PCI Express® link training, a link is established which is suitable for communication between both sides, i.e. host controller (e.g. SX2-SLIDE) and target side adapter. The link width can vary between 1 - 2 - 4, and the data transfer rate may be either 2.5GT/s (Gen1) or 5GT/s (Gen2).

PCIe x 4 Connector

Front Panel Connector PCIe x 4
EKF Parts #255.3.4.038.00 (Receptacle) & 255.3.4.138.00 (Guide Frame)

PCIe x 4



Part #255.3.4.038.00 & 255.3.4.138.00
draft - do not scale • © EKF • ekf.com

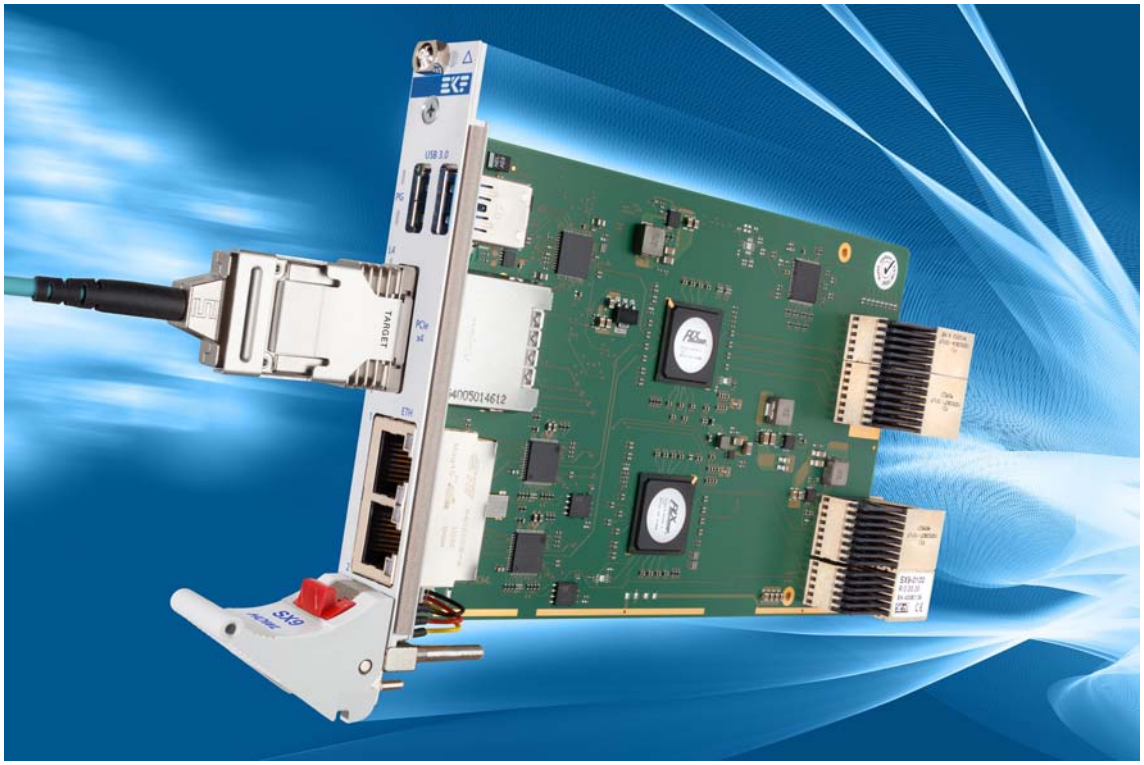
GND	A1	B1	GND
PETp0	A2	B2	PERp0
PETn0	A3	B3	PERn0
GND	A4	B4	GND
PETp1	A5	B5	PERp1
PETn1	A6	B6	PERn1
GND	A7	B7	GND
PETp2	A8	B8	PERp2
PETn2	A9	B9	PERn2
GND	A10	B10	GND
PETp3	A11	B11	PERp3
PETn3	A12	B12	PERn3
GND	A13	B13	GND
CREFCLKp	A14	B14	PWR +3.3V
CREFCLKn	A15	B15	PWR +3.3V
GND	A16	B16	PWR_RTN 1)
SB_RTN 2)	A17	B17	PWR_RTN 1)
CPRSNT# 3)	A18	B18	CWAKE# 3)
CPWRON 4)	A19	B19	CPERST# 4)

PWR +3.3V - protected by on-board PolyFuse 1.5A

For signal descriptions please refer to PCI Express External Cabling Specification Rev. 2.0

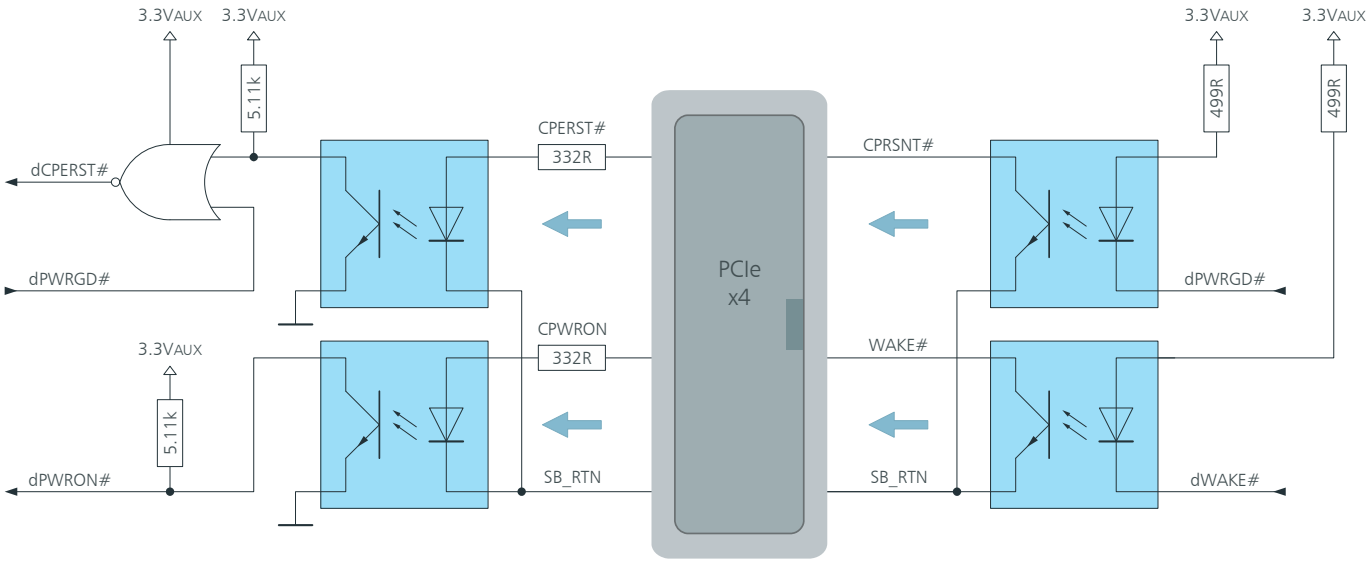
1) connected to GND
2) Sideband reference, isolated from GND
3) Output from Downstream System (Target) to Upstream System (Host)
   Isolated via photocoupler TLP281
4) Input from Upstream System (Host) to Downstream System (Target)
   Isolated via photocoupler TLP281

PCIe x 4 Cable Assemblies	
255.3.4.938.0.020	PCIe x 4 external cable assembly, 38-circuit, 2m
255.3.4.938.0.040	PCIe x 4 external cable assembly, 38-circuit, 4m
255.3.4.938.0.050	PCIe x 4 external cable assembly, 38-circuit, 5m
255.3.4.938.0.070	PCIe x 4 external cable assembly, 38-circuit, 7m
255.3.4.938.8.0100	PCIe x 4 external active optical cable assembly, 10m
other configurations on request	

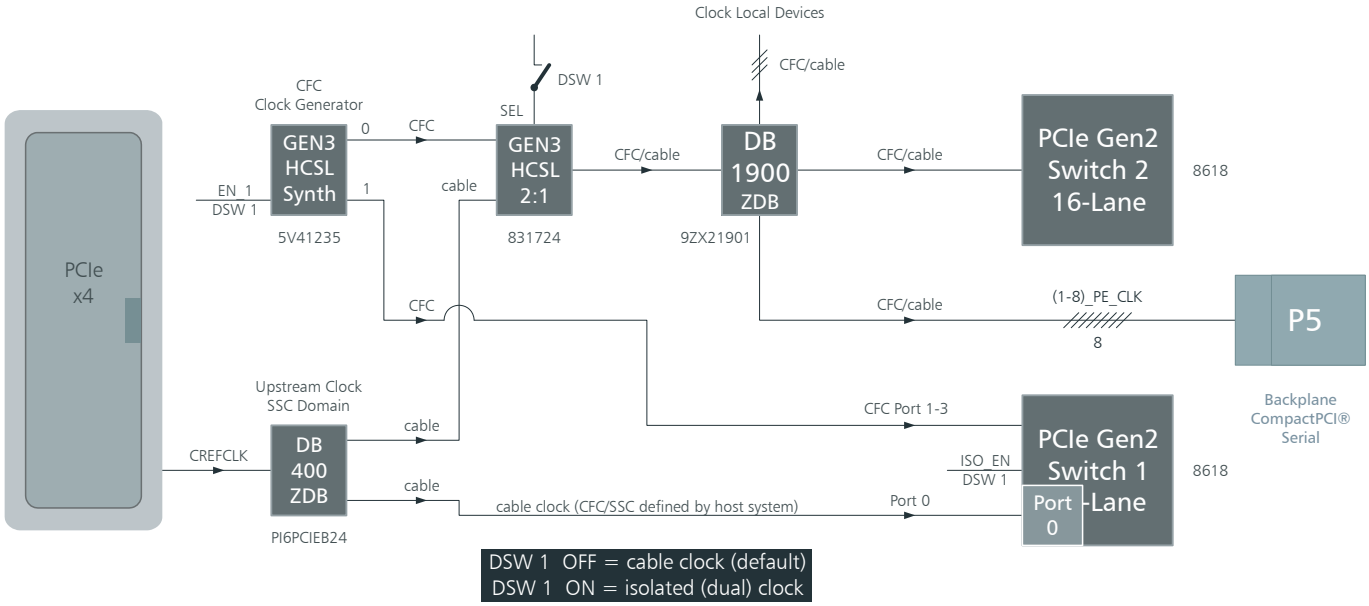


SX9-HOWL w. AOC

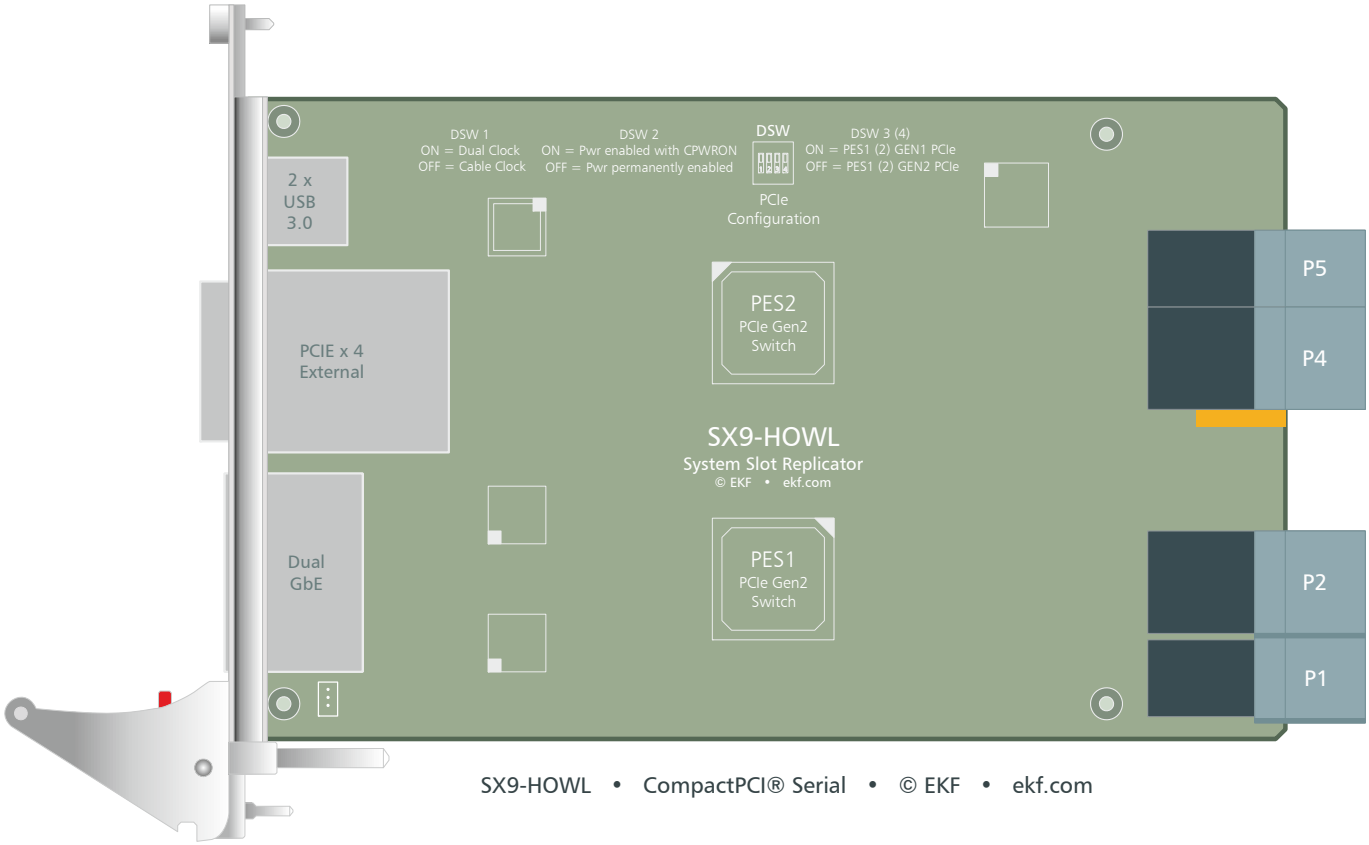
Power-Domain Isolation SX* Target Adapters (Downstream Subsystem) • © EKF



SX9-HOWL Dual Clocking Support • © EKF

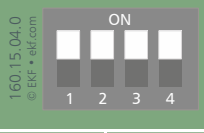


PCI Express® Setup



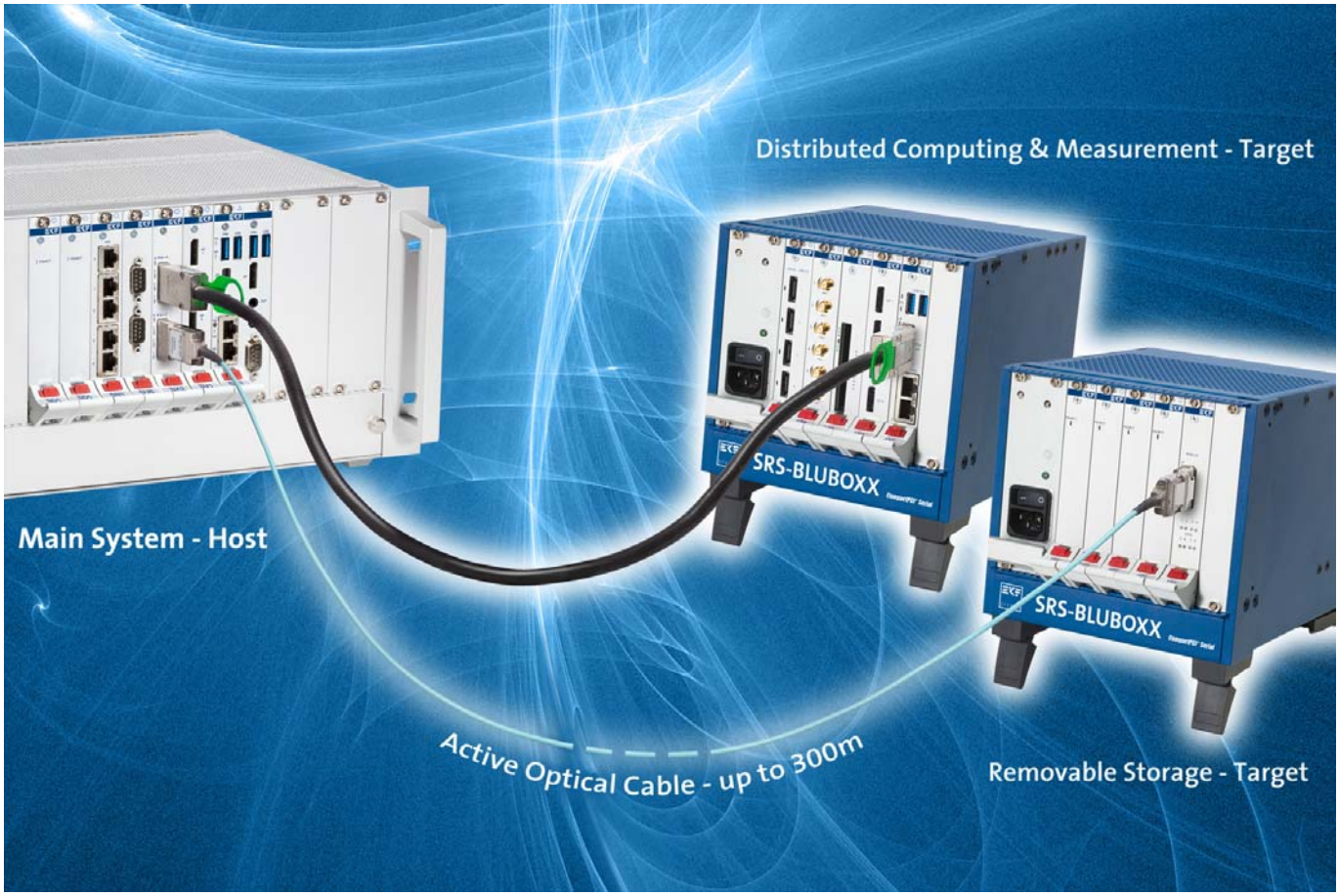
SX9-HOWL • CompactPCI® Serial • © EKF • ekf.com

Dip Switch DSW Setup



1	2	3	4
ON = dual clock on-board clock is isolated from PCIe cable clock, on-board CFC synthesizer is in use instead, to be used with SSC cable clock only	**ON = power control through CPWRON** default CPWRON is a PCIe cable sideband signal, controlled by the host (upstream system)	**ON = PES1 GEN1** forces PCIe Switch 1 to Gen1 transfer rate refer to block diagram for links/lanes affected	**ON = PES2 GEN1** forces PCIe Switch 2 to Gen1 transfer rate refer to block diagram for links/lanes affected
Off = cable clock default PCIe cable clock is also used on-board, either CFC or SSC, dependent from host (upstream system)	**Off = power permanently enabled** host not involved to enable local voltage regulators	**OFF = PES1 GEN2** default allows PCIe Switch 1 to operate with either Gen1 or Gen2 transfer rate, dependent from the host system capability	**OFF = PES2 GEN2** default allows PCIe Switch 2 to operate with either Gen1 or Gen2 transfer rate, dependent from PES1 settings

Typical Application



For distances up to 300m between host system and target system active optical cables (AOC) are recommended. Below 7m (e.g. when connecting racks in a common enclosure) a low cost copper cable is sufficient. Please note, that an AOC employs a host side connector and a target side connector, which must not be interchanged. A PCI Express® copper cable however is configured identical at both endings. While a copper cable is spread spectrum clock (SSC) compatible, the AOC requires a constant frequency clock (CFC). For proper operation over AOC, setup the host interface (e.g. SX2-SLIDE) for CFC.

Active Optical Cable Connector

Copper Cable Connector

Power Sequencing

Please understand, that host and connected target hardware should be considered as distributed parts of a common computer system. During BIOS POST the whole system will be explored for PCI Express® devices attached to the PCIe® root complex (processor on host system CPU card). Devices which are not active (powered up) at this time, will not be enumerated by the BIOS and are consequently not available for the operating system afterwards.

Hence a power sequencing procedure must be observed for host system and target system. The rule is simple: Power up the target system before the host system, or simultaneously. If power sequencing conditions cannot be maintained, the host system must be restarted again, until the remote target devices are visible to the host CPU.

If the host system is equipped with an EKF processor board such as the SC3-LARGO or higher, a startup time delay up to 12s can be configured via BIOS setup:

Setup (F2): Advanced -> Miscellaneous Configuration -> Execute Delay after Reset

The adjusted delay would be executed before enumeration and initialization of PCI Express® devices, thus permitting a reasonable power up time lag for the remote target system. The delay countdown is indicated by a red blinking LED GP in the CPU card front panel.

P1/P2 CompactPCI® Serial System Slot Backplane Connectors

P2 CompactPCI® Serial System Slot Backplane Connector

EKF Part #250.3.1208.20.00 • 96 pos. 12x8, 16mm Width

P2	A	B	C	D	E	F	G	H	I	J	K	L
8	GND	IO	IO	GND	2_ USB2+	2_ USB2-	GND	3_ USB2+	3_ USB2-	IO	4_ USB2+	4_ USB2-
7	IO	IO	GND	IO	IO	GND	IO	IO	GND	IO	IO	GND
6	GND	2_PE TX06+	2_PE TX06-	GND	2_PE RX06+	2_PE RX06-	GND	2_PE TX07+	2_PE TX07-	GND	2_PE RX07+	2_PE RX07-
5	2_PE TX04+	2_PE TX04-	GND	2_PE RX04+	2_PE RX04-	GND	2_PE TX05+	2_PE TX05-	GND	2_PE RX05+	2_PE RX05-	GND
4	GND	2_PE TX02+	2_PE TX02-	GND	2_PE RX02+	2_PE RX02+	GND	2_PE TX03+	2_PE TX03-	GND	2_PE RX03+	2_PE RX03-
3	2_PE TX00+	2_PE TX00-	GND	2_PE RX00+	2_PERX 00-	GND	2_PE TX01+	2_PE TX01-	GND	2_PE RX01+	2_PE RX01-	GND
2	GND	1_PE TX06+	1_PE TX06-	GND	1_PE RX06+	1_PE RX06-	GND	1_PE TX07+	1_PE TX07-	GND	1_PE RX07+	1_PE RX07-
1	1_PE TX04+	1_PE TX04-	GND	1_PE RX04+	1_PE RX04-	GND	1_PE TX05+	1_PE TX05-	GND	1_PE RX05+	1_PE RX05-	GND

P1 CompactPCI® Serial System Slot Backplane Connector

EKF Part #250.3.1206.20.02 • 72 pos. 12x6, 14mm Width

P1	A	B	C	D	E	F	G	H	I	J	K	L
6	GND	1_PE TX02+	1_PE TX02-	GND	1_PE RX02+	1_PE RX02-	GND	1_PE TX03+	1_PE TX03-	GND	1_PE RX03+	1_PE RX03-
5	1_PE TX00+	1_PE TX00-	GND	1_PE RX00+	1_PE RX00-	GND	1_PE TX01+	1_PE TX01-	GND	1_PE RX01+	1_PE RX01-	GND
4	GND	1_ USB2+	1_ USB2-	GND	RSV	RSV	GND	1_SATA TX+	1_SATA TX-	GND	1_SATA RX+	1_SATA RX-
3	1_USB3 TX+	1_USB3 TX-	PWR BTN#	1_USB3 RX+	1_USB3 RX-	PWR_ FAIL#	SATA SDI	SATA SDO	GND GA2	SATA SCL	SATA SL	GND GA3
2	GND	I2C SCL	I2C SDA	GND	GND PS_ON#	RST#	GND	PRST#	WAKE#	GND	RSV	SYS EN#
1	+12V	STBY	GND	+12V	+12V	GND	+12V	+12V	GND	+12V	+12V	GND

pin positions printed gray: not connected or PU terminated

For signal descriptions please refer to PICMG CPCI-S.0 R1.0 CompactPCI® Serial Specification

P4/P5 CompactPCI® Serial System Slot Backplane Connectors

P5 CompactPCI® Serial Peripheral Slot Backplane Connector

EKF Part #250.3.1206.20.00 • 72 pos. 12x6, 12mm Width

P5	A	B	C	D	E	F	G	H	I	J	K	L
6	5_PE CLKE#	5_PE CLK+	5_PE CLK-	6_PE CLKE#	6_PE CLK+	6_PE CLK-	7_PE CLKE#	7_PE CLK+	7_PE CLK-	8_PE CLKE#	8_PE CLK+	8_PE CLK-
5	1_PE CLK+	1_PE CKL-	1_PE CLKE#	2_PE CLK+	2_PE CKL-	2_PE CLKE#	3_PE CLK+	3_PE CKL-	3_PE CLKE#	4_PE CLK+	4_PE CKL-	4_PE CLKE#
4	GND	8_PE TX02+	8_PE TX02-	GND	8_PE RX02+	8_PE RX02-	GND	8_PE TX03+	8_PE TX03-	GND	8_PE RX03+	8_PE RX03-
3	8_PE TX00+	8_PE TX00-	GND	8_PE RX00+	8_PE RX00-	GND	8_PE TX01+	8_PE TX01-	GND	8_PE RX01+	8_PE RX01-	GND
2	GND	7_PE TX02+	7_PE TX02-	GND	7_PE RX02+	7_PE RX02-	GND	7_PE TX03+	7_PE TX03-	GND	7_PE RX03+	7_PE RX03-
1	7_PE TX00+	7_PE TX00-	GND	7_PE RX00+	7_PE RX00-	GND	7_PE TX01+	7_PE TX01-	GND	7_PE RX01+	7_PE RX01-	GND

P4 CompactPCI® Serial Peripheral Slot Backplane Connector

EKF Part #250.3.1208.20.00 • 96 pos. 12x8, 16mm Width

P4	A	B	C	D	E	F	G	H	I	J	K	L
8	GND	6_PE TX02+	6_PE TX02-	GND	6_PE RX02+	6_PE RX02-	GND	6_PE TX03+	6_PE TX03-	GND	6_PE RX03+	6_PE RX03-
7	6_PE TX00+	6_PE TX00-	GND	6_PE RX00+	6_PE RX00-	GND	6_PE TX01+	6_PE TX01-	GND	6_PE RX01+	6_PE RX01-	GND
6	GND	5_PE TX02+	5_PE TX02-	GND	5_PE RX02+	5_PE RX02-	GND	5_PE TX03+	5_PE TX03-	GND	5_PE RX03+	5_PE RX03-
5	5_PE TX00+	5_PE TX00-	GND	5_PE RX00+	5_PE RX00-	GND	5_PE TX01+	5_PE TX01-	GND	5_PE RX01+	5_PE RX01-	GND
4	GND	4_PE TX02+	4_PE TX02-	GND	4_PE RX02+	4_PE RX02+	GND	4_PE TX03+	4_PE TX03-	GND	4_PE RX03+	4_PE RX03-
3	4_PE TX00+	4_PE TX00-	GND	4_PE RX00+	4_PE RX00-	GND	4_PE TX01+	4_PE TX01-	GND	4_PE RX01+	4_PE RX01-	GND
2	GND	3_PE TX02+	3_PE TX02-	GND	3_PE RX02+	3_PE RX02-	GND	3_PE TX03+	3_PE TX03-	GND	3_PE RX03+	3_PE RX03-
1	3_PE TX00+	3_PE TX00-	GND	3_PE RX00+	3_PE RX00-	GND	3_PE TX01+	3_PE TX01-	GND	3_PE RX01+	3_PE RX01-	GND

pin positions printed gray: not connected

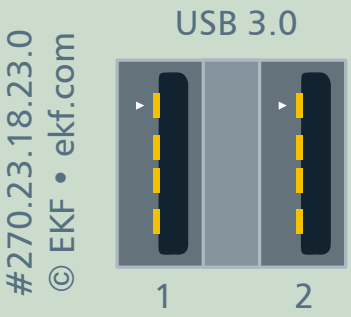
For signal descriptions please refer to PICMG CPCI-S.0 R1.0 CompactPCI® Serial Specification

USB 3.0 Connectors (Option)

As an option, the SX9-HOWL is equipped with a dual front panel receptacle, which can accommodate two USB 3.0 or USB 2.0 type A cable connectors (USB root hub). When connected to USB 2.0 compliant devices, only the classic 4 contacts (data pair, +5V and GND) are in use. USB 3.0 devices in addition communicate via the SuperSpeed differential transmit and receive signal pairs, available across another 5 contact pins.

The front panel USB jacks are tied to an on-board PCI Express® to USB 3.0 controller (TUSB7320 or TUSB7340). For some operating systems e.g. Windows® 7, installation of a xHCI driver would be required to enable the SuperSpeed mode (download via www.ti.com).

USB • Dual USB 3.0 Receptacle
USB 3.0 dual type A receptacle, stacked, 18-position (270.23.18.2)



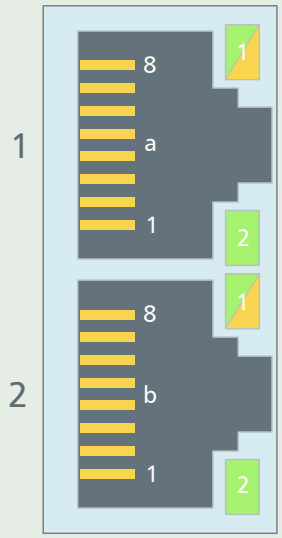
1	VBUS +5V 1.5Amax
2	USB D-
3	USB D+
4	GND
5	SS RX-
6	SS RX+
7	GND
8	SS TX-
9	SS TX+

Each connector provides +5V (VBUS) for powering external devices. A dual-channel electronic power switch (TPS2060) is used on the SX9-HOWL which limits the maximum output current of each individual USB connector to a safe level. The USB power switch is rated at >2A current limit typically, which is suitable even for applications where heavy capacitive loads are likely to be encountered, e.g. VBUS powered USB disk drives. The electronic switch is enabled by the on-board USB controller (i.e. it is managed by the driver software). Front panel LEDs labelled 1 and 2 signal the power-on state individually for each USB receptacle.

Gigabit Ethernet Jacks (Option)

As an option, the SX9-HOWL is provided with two independent PCIe to Gigabit Ethernet Controllers (Intel® I210). Associated are two RJ45 front panel jacks. Driver download may be required prior to use - please refer to the Intel® Website.

Gigabit Ethernet
270.02.08.5 Dual RJ45 Jack



LED 1
yellow=1Gbps green=100Mbps off=10Mbps
LED 2
green=link established blinking=activity

Ports		
1-2	1	MDX0+
	2	MDX0-
	3	MDX1+
	4	MDX2+
	5	MDX2-
	6	MDX1-
	7	MDX3+
	8	MDX3-

I210 Gigabit Ethernet Controller Feature Summary

- Two independent Gigabit Ethernet controllers (2 x MAC address) Intel® I210IT
- Integrated PHYs 1000BASE-T, 100BASE-TX, 10BASE-T (IEEE 802.3, 802.3u, 802.3ab)
- IEEE 802.3ab Auto Negotiation for automatic link configuration
- Auto MDI, MDI-X Crossover at all speeds
- Full duplex operation at 10/100/1000Mbps
- 9.5KB Jumbo Frame support
- Hardware-based time stamping (IEEE 1588) and support for 802.1AS - Precise Timing Protocol
- Support for Energy Efficient Ethernet (EEE) standard of IEEE 802.3az
- Option IEEE 802.1Qav compliant Audio-Video Bridging (AVB)
- IPv4, IPv6, TCP/UDP checksum offloads
- Driver support for all major operating systems
- Two front panel connectors RJ45 with integrated magnetics

Related Documents

Similar Cards Using PCIe External Cabling	
SX2-SLIDE	CompactPCI® Serial • PCIe External Cabling • Host Side Dual Gen2 x4 www.ekf.com/s/sx2/sx2.html
SX5-STREAM	CompactPCI® Serial • PCIe External Cabling • Host Side Dual Gen3 x8 www.ekf.com/s/sx5/sx5.html
SXC-LOOP	CompactPCI® Serial • PCIe External Cabling • Target Side Gen3 x8 • PCIe System Slot Replicator 2 x Gen3 x8 Fat Pipe Slots www.ekf.com/s/sxc/sxc.html
SXS-STRING	CompactPCI® Serial • PCIe External Cabling • Target Side Gen2 x4 • 8-Port SATA RAID www.ekf.com/s/sxs/sxs.html
DC2-STAG	XMC Mezzanine Module • PCIe External Cabling • Host Side Dual Gen2 x4 http://www.ekf.com/d/dpxc/dc2/dc2.html

Reference Documents		
Term	Document	Origin
CompactPCI® Serial	CPCI-S.0	www.picmg.org
PCI Express®	PCI Express® External Cabling Specification 2.0	www.pcisig.com
USB	USB 3.0 Universal Serial Bus Specification (SuperSpeed)	www.usb.org
xHCI	eXtensible Host Controller Interface for Universal Serial Bus (xHCI) Rev. 1.0 2010-05-21	www.intel.com

Ordering Information

Ordering Information
For popular SX9-HOWL SKUs please refer to www.ekf.com/liste/liste_21.html#SX9

Industrial Computers Made in Germany

boards. systems. solutions.

EKF Elektronik GmbH
Philipp-Reis-Str. 4 (Haus 1)
Lilienthalstr. 2 (Haus 2)
59065 HAMM
Germany

Phone +49 (0)2381/6890-0
Fax +49 (0)2381/6890-90
Internet www.ekf.com
E-Mail sales@ekf.com